Electric field modulation of spin and charge transport in two dimensional materials and complex oxide hybrids

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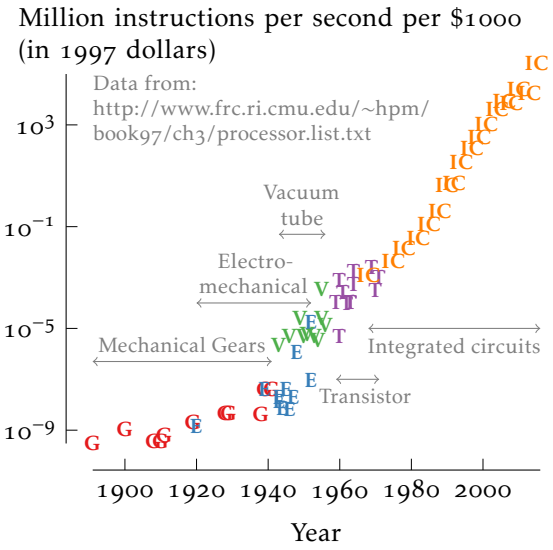
INTRODUCTION

ABSTRACT

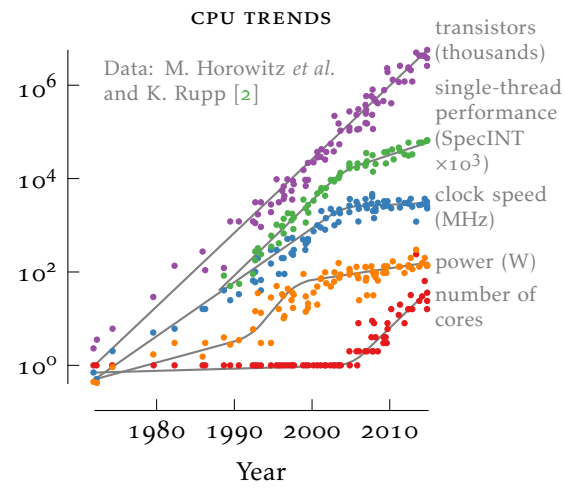
In the past hundred years the required cost and power per computation saw an exponential decrease. This decrease was made possible by different computational devices such as: mechanical gears and vacuum tubes. Since 1965 we are in the era of the integrated circuits. However, since the turn of the twentieth century integrated circuits are encountering more and more problems. The problems are mainly due to increased heat development from ever shrinking devices. In order to overcome the heating issues, manufacturers are looking at alternative materials and alternatives to current CMOS devices. A promising low power option is that of spintronics, which also uses the spin of an electron next to its charge for logic operations.

1.1 THE EVER SHRINKING CALCULATORS

During the twentieth century computational speeds increased dramatically, while at the same time the price per calculation dropped, as shown on the right with data redrawn from [1, chapter 3]. At the start of the century, mechanical gears slightly increased the computational speed as compared to manual calculations. In the following decades this technology was improved as it matured. Simultaneously new technologies were invented, such as the electromechanical calculators, which eventually took over as they became cheaper and faster. This process would repeat itself several times over.



Currently we are in the era of the integrated circuits, which started in the 1960s. During the early days of integrated circuits it was Gordon Moore who noted that the number of transistors on a chip grew exponentially with time, due to the downscaling of the transistor's feature sizes. As a result, the number of transistors doubled about every 2 years, without affecting the chip area [3]. This transistor growth is shown on the right. The relationship became known as Moore's law, which still holds true today



As feature sizes shrank, fabrication became increasingly challenging and expensive [4, figure 1.1.14]. As the complexity rose, efforts of researchers, designers, production facilities etc. needed to be coordinated. For this purpose various road maps were constructed, starting in the 1990s [5, 6]. These maps basically followed Moore's law and from there determined the feature sizes for the next generation of processors. The road maps gave everyone involved in the development of the next generation tools and techniques for smaller and faster integrated circuits a clear goal to work towards.

However, since the turn of the twentieth century the first challenges presented themselves, as can be seen in the graph above. Starting in the 1990s the power consumption went up rapidly and later became a problem as the central processing unit's (CPU) temperatures became too hot around the year 2000. In order to curb the increasing power consumption/heat generation, the CPU's clock speed was no longer increased, but instead the workload was divided among several different

cores. Note that despite the constant clock speeds, the performance of a single transistor (single-thread) still increased, albeit not as rapidly as pre-2000. Despite all the problems, manufacturers are still pushing for smaller feature sizes [7].

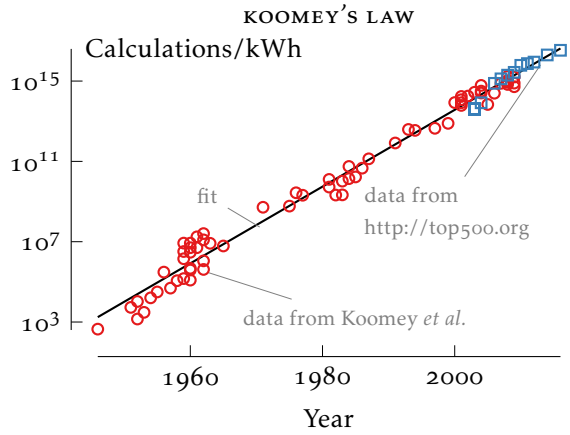
The jump in power consumption was due to the fact that the so called Dennard scaling broke down [8, 9]. Dennard scaling states that the energy consumption of a transistor can be kept constant by scaling each component accordingly. The power consumption P of a transistor is given by $P = NfCV^2$, where N is the number of transistors, f is the clock speed, C is the capacitance and V is the turn-on voltage. In order to quantify the scaling between successive generations, a scaling factor S is introduced, which is $S = 32/22 = 1.45$ when going from 32 to 22 nm. Each parameter then scales as follows: the number of transistors scales with S^2, since they are laid out in two dimensions (although this is changing [10]); the capacitance scales with S^{-1}, since the gate area A and thickness t scale with $A \propto S^{-2}$ and $t \propto S^{-1}$ respectively, causing $C \propto A/t = S^{-2}/S^{-1} = S^{-1}$; the reduction in gate insulator thickness leads to a lower turn-on voltage $V^2 \propto S^{-2}$; and because the RC time of the system has deceased, the frequency can be scaled according to S. Thus $P_{\text{scaling}} = S^{-2}SS^{-1}(S^{-1})^2 = 1$ and the power consumption of a transistor was unaffected.

The breakdown of Dennard scaling was due to the fact that devices, and particularly the gate insulator thickness and gate length, got so small that electrons could tunnel through these barriers. These tunnelling electrons caused large leakage currents in the off-state of the transistor. Due to the increasing leakage currents the turn-on voltage could not be decreased, as doing so would exponentially decrease the difference between the on- and off-state. As a consequence the power consumption of each successive generation increased by S^2 [9].

1.2 SILICON'S SUCCESSOR

In order to circumvent leakage currents and consequently heating, manufacturers are looking for alternatives to silicon. For example, to prevent electrons from tunnelling through the gate dielectric, manufacturers started using so-called high-k dielectrics [11]. By using hafnium dioxide (HfO_2), for example, which has a dielectric constant 4-6 times that of SiO_2, the thickness t of the dielectric can be increased (thereby exponentially decreasing the tunnelling current), without compromising the capacitance since $C \propto \epsilon/t$.

Due to these advances, more and more calculations could be performed with the same amount of energy despite the breakdown of Dennard scaling, as shown on the right. This trend was spotted by Koomey *et al.* and has been dubbed Koomey's law [12]. The points marked as ○ were taken from Koomey *et al.* and contain data on a variety of personal and super computers. To this I have added the most energy efficient super computers and these are plotted as □.



For future generations this trend will likely continue, as the current materials reach their limits. Possible materials which can succeed silicon and other parts of the integrated circuits are two-dimensional (2D) materials and complex oxides. Both materials are used for the research in this thesis for different reasons.

First I will discuss the 2D materials. As the name suggests, these materials are purely 2D and only a single atom thick. After the isolation of the first 2D material, carbon's 2D allotrope graphene, a whole class of 2D materials was isolated. Their electrical properties vary from conducting to insulating and often vary with the number of layers. As an example MoS_2 is a direct 1.9 eV bandgap semiconductor in single layer form, but becomes an indirect semiconductor from two layers and up. Moreover the bandgap reduces gradually towards a bulk value of 1.3 eV [13]. These varying electrical properties of 2D materials, which can replace all the parts in a transistor, is just one advantage of these materials. Other attractive features are the fact that they can form continuous layers of the lowest possible thickness–a single atom. Finally, because of their limited thickness these materials can be used to make flexible and transparent devices.

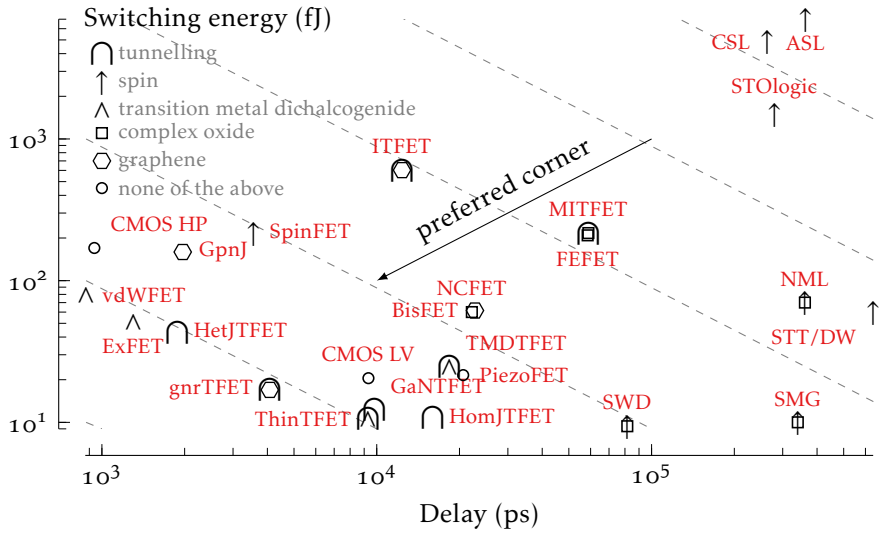
The second material class is the complex oxides and more specifically for this thesis, insulating $SrTiO_3$ and semiconducting Nb-doped $SrTiO_3$. Complex oxides often have electric and magnetic properties which can often be highly influenced by external parameters such as strain, electric field and temperature. The sensitivity to these parameters is due to the strong electron correlations from orbital overlap. These correlations result in complex physics where charge, spin and orbital filling/overlap strongly influence each other. As a result of these strong electron correlations it offers the unique possibility of modulating the electric or magnetic properties in complex oxide based devices. For example, $SrTiO_3$ has a dielectric permittivity which is 100 times as large as SiO_2 at room temperature and highly depends on temperature and electric field.

1.3 ALTERNATIVE TECHNOLOGIES

However replacing the current materials will probably only delay the demise of current CMOS technology. Therefore great efforts are undertaken to find the successor of CMOS. So far there are many alternative logic device architectures which provide a significant improvement in different areas over current CMOS [14, 15].

In order to compare alternative technologies, different metrics can be used. On metric to track is the switching energy versus delay of a logic unit, as shown below in a redrawn graph from Nikonov *et al.* [15]. The energy and delay were estimated by Nikonov *et al.* by using a simple analytical model of the components. Note the widespread in performance between different technologies. The technologies which are based on concepts or materials relevant for this thesis use special symbols. If multiple concepts/materials are used the symbols are superimposed. In this graph only several (Tunnelling) Field Effect Transistor ((T)FET)-based logic devices offer an advantage over the current, highly optimised, CMOS technology.

32-BIT ARITHMETIC LOGIC UNIT USING DIFFERENT FOLLOW UP TECHNOLOGIES

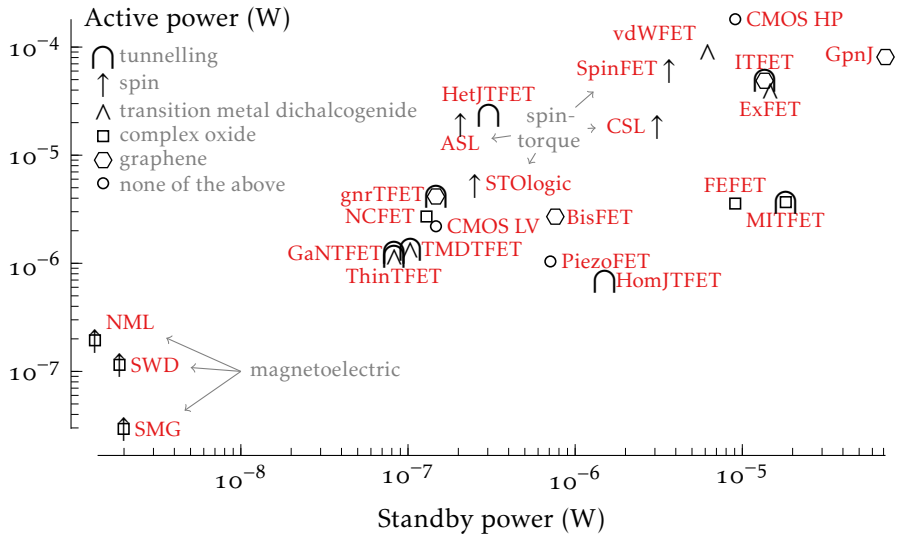


The abbreviations are as follows: Complementary metal–oxide–semiconductor high performance (CMOS HP), CMOS low voltage (CMOS LV), van der Waals Field Effect Transistor (vdWFET), Homojunction III-V Tunnelling FET (HomJTFET), Heterojunction III-V TFET (HetJTFET), Graphene Nanoribbon TFET (gnrTFET), Interlayer TFET (ITFET), 2D Heterojunction Interlayer TFET (ThinTFET), GaN TFET (GaNTFET), Transition Metal Dichalcogenide TFET (TMDTFET), Graphene pn-Junction (GpnJ), Ferroelectric FET (FEFET), Negative Capacitance FET (NCFET), Piezoelectric FET (PiezoFET), Bilayer Pseudospin FET (BisFET), Excitonic FET (ExFET), Metal-Insulator TFET (MITFET), Sughara-Tanaka SpinFET, All Spin Logic (ASL), Charge-Spin Logic (CSL), Spin Torque Domain Wall (STT/DW), Spin Majority Gate (SMG), Spin Torque Oscillator (STOlogic), Spin Wave Device (SWD) and Nanomagnetic Logic (NML).

The purpose of this overview is to show there are many alternative ideas, each with their own strengths and weaknesses. Also the exact switching energy and delays are subject to discussion. The differences were earlier shown by the authors in reference [14, figure 51], where they compare their results with those of the 2011 NRI benchmark. Furthermore the materials which are used are often not set in stone, but give an idea of the possibilities.

Another important pair of metrics to track are the on and off power of a device, which is shown below as redrawn data from reference [15]. From this overview it is clear that magnetoelectric (voltage-driven) spintronic devices are several orders of magnitude better than other contenders, especially in standby power. The reason for the low standby power is that the nanomagnets in these spintronic devices are non-volatile and power can be turned off when the magnets do not need to be switched. In theory there can be zero power consumption, however a transistor is still required to turn the circuit on and off. Another potential advantage of spintronics is that spin currents in principle do not require a (Joule heat generating) charge current. However, the technologies in this graph do not utilise this property. Nonetheless it is clear that spintronics provide a valuable alternative for certain applications where switching speed is not important, but power consumption is. Examples of these applications include devices which rely on battery power, such as wearable electronics or remote sensors with sporadic activity.

32-BIT ARITHMETIC LOGIC UNIT USING DIFFERENT FOLLOW UP TECHNOLOGIES



1.4 GRAPHENE SPINTRONICS

It is clear that spintronic based devices offer several advantages over other technologies. In order to fabricate a successful spintronic device there are several prerequisites. This boils down to a few important steps: 1) the generation of a spin imbalance inside a channel; 2) maintaining the imbalance while the spins are transported, while possibly manipulating the spins for logic operations and; 3) detecting the spin imbalance.

A very promising material to fabricate spintransport channels from is graphene. At room temperature it has longer spin relaxation lengths and times then most metals and semiconductors [16, table 2]. However, it was predicted that graphene should have an even longer spin relaxation length.

In order to find the origin of the discrepancy between the predictions and experiments, many variables are investigated such as: the encapsulation of graphene [17] and improving the quality of the contacts [18]. In order to contribute to these efforts, we investigate spin transport through graphene in a high dielectric constant environment in chapter 4 and we investigate the possibility of using two-dimensional MoS_2 as tunnel barriers in chapter 6.

1.5 COMPLEX OXIDE SPINTRONICS

Another promising material for spintronics are the complex oxides and more specifically for this thesis: Nb-doped $SrTiO_3$. While Nb:$SrTiO_3$ can not match graphene's spin lifetimes, it certainly provides an interesting playground for spintronic applications [19]. The fact that it has a dielectric constant which varies with both temperature and electric field, allows us to electrically control the type of spin which transmits through the interface as we show in chapter 5.

Furthermore there are many complex oxides available with a wide range of material properties such as: ferroelectricity, ferromagnetism, piezoelectricy and super conductivity. Since these materials can easily be integrated with each other, this leads to a wide range of possible device geometries such as: resistive RAM, ferroelectric RAM, oxide spintronics, multiferroic devices and memristors [20–24].

1.6 OUTLOOK

Predicting the next technology and the future in general is always difficult, but given the current status we can give a reasonable outlook. From the previous sections it is clear that there are many potential follow-up technologies, despite omitting many (premature) concepts. Also the shown technologies are relatively compatible with integrated circuits and probably relatively easy to incorporate with current technologies. Based on this I would expect to see some of these technologies to be integrated into devices in the coming 5 years.

Since there is such a wide spread in device metrics such as the performance and energy consumption, many expect different concepts to be used in specialised chips for certain purposes [25, 26]. The change in perspective was also the reason why the International Technology Roadmap for Semiconductors [5], was rebooted in May 2016 and renamed into IEEE Rebooting Computing Initiative (RCI) and the International Roadmap for Devices and Systems (IRDS) [26]. These new roadmaps do not focus on following Moore's law, but instead diversify into different technologies

for specific applications. Examples from the initiative include: adiabatic/reversible computing which could enable far lower power consumption; neuromorphic computing for recognition problems; and memory-centric computing for a closer integration of memory and processor to prevent the shuffling of information back and forth.

Although the initiative is quite recent, diversification of chips is not. The gaming industry has mainly been responsible for the large demand of specialised chips which focus on graphics processing. These chips are optimised for large amounts of parallel processing. On the other hand, also the central processing unit (CPU) has many varieties: from low power, relatively slow CPU's for mobile phones and embedded devices, to high performance CPU's for servers.

Alternatively it is also possible that if further improvements to integrated circuits get too expensive we will see a new technology take over. This is also what we saw in section 1.1 which started with mechanical gear calculators and ended with the integrated circuits we see today. Perhaps the next computational technology will be quantum computers [27], bio inspired computing [28] or DNA computing [29].

1.7 THESIS OUTLINE

This thesis is build up into two parts. In the first part I will discuss background information which is needed to understand most concepts in this thesis. Then in chapter 2 I will first go into the theoretical background behind the experiments and different materials which are used. In chapter 3 I will treat the experimental concepts, such as device fabrication and how the measurements are performed.

Then in the second part of the thesis I will discuss the experimental results:

- In chapter 4 I will describe the results of non-local spin transport measurements in graphene on an insulating $SrTiO_3$ substrate. $SrTiO_3$ has a dielectric permitivity which is much higher that that of SiO_2 and furthermore increases by two orders of magnitude at low temperature. By performing temperature dependent spin transport measurements, we try to understand the influence of a high dielectric permittivity environment on the spin transport in graphene.

- Chapter 5 describes spin accumulation in semiconducting Nb-doped $SrTiO_3$. Here we find that while cooling down the sign of the spin signal decreases and becomes negative around 130 K. Additionally below 130 K the sign can also be reversed by tuning the electric field at the interface (through the applied bias). We attribute this behaviour to the highly non-linear dielectric permittivity of Nb-doped $SrTiO_3$, which changes the spin polarisation of the injection electrons via alteration of the tunnel barrier shape.

- In chapter 6 we investigate the possibility to use two-dimensional semiconducting MoS_2 as a tunable tunnel barrier between graphene and a metal electrode. We find that the barrier shows tunnelling characteristics and a moderate tunability of the barrier resistance with gate voltage.

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